MIPS 4K/5K™ Lead Vehicle Datasheet

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MIPS Technologies, Inc.
1225 Charleston Road
Mountain View, CA 94043-1353

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1 Introduction

This document contains the user level documentation for the MIPS 4K and 5K lead vehicle chips. The lead vehicle (called “LV” throughout the rest of this document) is a testchip specified by MIPS which all core licensees must produce in order to allow testing of silicon functionality.

This document does not describe the internal details of the 4K & 5K microprocessor cores, it only concentrates on the issues relevant for using the LV chips in a hardware design process, e.g. pinout, bus protocols, timing etc.

In most aspects relevant for this document, the LV chips for 4K & 5K cores are identical, as the package, pinout and bus protocol employed is the same. In situations where a difference exists, it will be clearly noted.

For detailed information on silicon specific data for a particular LV, a “Specification Update” document is issued for each. These documents are the definitive source of information regarding a specific LV implementation, and both this general datasheet as well as the specification update must be read in order to obtain the complete set of relevant information.

1.1 Main Features

Most of the features in the 4K & 5K LVs are identical:

- LV is a fully equipped chip which is usable for both evaluation purposes and real designs
- Supports industry standard SysAD64 bus protocol
- Built-in PLL to generate core clock from bus clock
- Supports core bond-out mode for SOC development applications
- BGA package with 388 balls
- Separate I/O and core supplies allows real-time power measurements
- All I/Os are 3.3V with TTL thresholds

The following tables describe the areas where there is a difference:

Table 1 Feature Differences (4K class LVs)

Feature	4K LV (4Kc/m)	4K LV (4Kp)	4KE, 4KS LV (4KEc/m, 4KSc)	4KE LV (4KEp)
Instruction set architecture	MIPS32	MIPS32	MIPS32	MIPS32
FPU included	No	No	No	No
Cache implementation	Write-Through	Write-Through	Write-Back	Write-Back
Cache set size	4 kByte	4 kByte	16 kByte	16 kByte
Associativity (I/D)	4I, 4D	4I, 4D	4I, 4D	4I, 4D
Total cache size (I/D)	16 kByte, 16 kByte	16 kByte, 16 kByte	64 kByte, 64kByte	64 kByte, 64 kByte
MMU	SW configurable: TLB, 16 dual entries OR Fixed mapping MMU	Fixed mapping MMU	SW configurable: TLB, 16 dual entries OR Fixed mapping MMU	Fixed mapping MMU
EJTAG	Version 2.5	Version 2.5	Version 2.6	Version 2.6

Table 1 Feature Differences (4K class LVs)

Feature	4K LV (4Kc/m)	4K LV (4Kp)	4KE, 4KS LV (4KEc/m, 4KSc)	4KE LV (4KEp)
PDtrace	Not available	Not available	Yes	Not available
PLL clock multipliers supported	2x, 3x, 4x 2x (RTL ver <= 3.2)	2x, 3x, 4x 2x (RTL ver <= 3.2)	2x, 3x, 4x	2x, 3x, 4x
Maximum core clock speed	Implementation dependent	Implementation dependent	Implementation dependent	Implementation dependent

Table 2 Feature Differences (5K class LVs)

Feature	5K LV (5Kc/m)	5K LV (5Kf)
Instruction set architecture	MIPS64	MIPS64
FPU included	No	Yes
Cache implementation	Write-Back	Write-Back
Cache set size	16 kByte	16 kByte
Associativity (I/D)	4I, 4D	4I, 4D
Total cache size (I/D)	64 kByte, 64 kByte	64 kByte, 64 kByte
MMU	SW configurable: TLB, 32 dual entries OR Fixed mapping MMU	SW configurable: TLB, 32 dual entries OR Fixed mapping MMU
EJTAG	Version 2.5 EJTAG version 2.6 in RTL ver. 2.2 or later	Version 2.6
PDtrace	Not available	Not available
PLL clock multipliers supported	2x, 3x, 4x	2x, 3x, 4x
Maximum core clock speed	Implementation dependent	Implementation dependent

Note that with regards to MMU functionality, there are two types of 4K and 4KE LVs. The first one implements the functionality of both the 4Kc and 4Km (4KEc, 4KEm) products (different MMUs). Which one to use is software configurable. This allows customers to get “two cores in one LV”, and The second type of 4K LV implements the 4Kp (4KEp) product, which only contains the fixed mapping MMU and the slow multiplier.

The clock multiplier support in 4K LVs is depending on the RTL version they are built on. Versions built using RTL version 3.2 or earlier supports only the 2x multiplier. Newer versions (RTL version 3.3 and later) support the full range of clock multipliers (2x, 3x, 4x). The RTL version for a specific LV is documented in the “Specification Update” document for that particular silicon. For 4KE and 4KS LV’s, all versions support the full set of clock multipliers.

For 5K LVs, all implement both the TLB style MMU and the fixed mapping MMU functionality, again software controllable.

For the 4KE, 4KS and 5K LVs, the indicated cache sizes are the maximum sizes supported. In some cases, implementations might implement smaller caches due to limitations in the available memory blocks. The actual implementation specific details are described in a later chapter and also in the "Specification update" document for that particular silicon.

Both 4K & 5K LVs allow the software to “down-size” the caches under software control, allowing eg. benchmarks to be run with different cache-sizes in order to determine the optimal cache size for the final application.

1.2 Dual Bus Modes

One of the main features of the LV chip is that it supports two bus modes: SysAD64 and core bond-out.

The SysAD64 protocol is a industry standard bus protocol which is employed by a wide range of MIPS processors from different vendors. North bridges supporting this bus protocol are also available from several sources.

When the chip is operating in core bond-out mode, the SysAD64 logic is disabled, and the ports on the microprocessor core is instead brought out on the physical LV pins. This allows customers to build a system employing the same bus protocol as they would when designing a real chip using a 4K or 5K core.

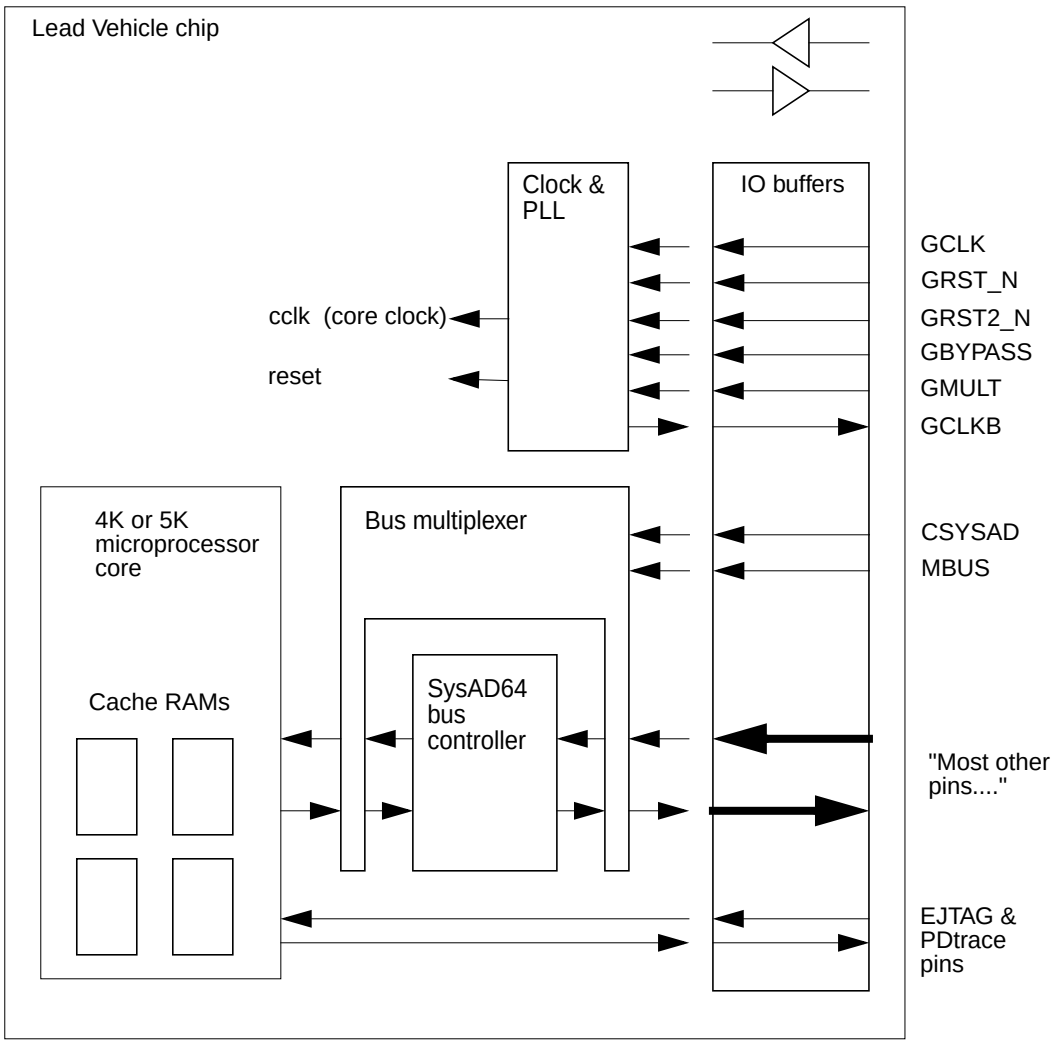

Figure 1 LV Block Diagram

The bus mode is controlled by the CSYSAD input pin which goes to the bus multiplexer. In order to save pins, many pins have two functions depending on the bus mode. This is described in detail in the pinout section.

2 Pin Description

This chapter describes the functional pinout of the LV, including a short description of each pin. The AC & DC characteristics and actual pinout on the package are both described in subsequent chapters.

The description is divided into three sections, one covering the shared pins which have identical functions in SysAD64 and bond-out mode, and two tables describing the multiplexed SysAD64 and bond-out mode pins which have different functionality in the two modes. Both the SysAD64 and bond-out mode tables are complete (describing all pins on the device) when seen together with the first table. Note that in the bond-out table, the physical pin name being used for a pin is always the SysAD64 name.

All pin names ending with _N have negative polarity, all others have positive polarity. A signal ending with "_N" is asserted or activated when driven low. Some pin names are inherited directly from the corresponding port names on the 4K and 5K cores. These pins do not necessarily follow the above naming convention.

Each pin type is listed as being either "I" (Input), "O" (Output) or "I/O" (Bidirectional pin). There are also a few 3S outputs, these are marked as "O (3S)".

2.1 Shared Pins with Identical Function in Both SysAD64 and Bond-out Mode

Table 3 Shared Function Pins

Global system level pins		
Pin name	**Type**	**Description**
GCLK	I	Master clock input. Normally this clock is used as a reference for the PLL in order to generate the internal core clock, and as such GCLK itself is the bus clock. In PLL bypass mode GCLK is directly used to drive the internal core clock. On the older 4K LVs, the PLL will always generate a 2x core clock. On newer 4K LVs and all 5K LVs, the multiplication factor is configurable (see GMULT pin description).
GCLKB	O	Outputs the internally generated bus clock which is 1/2, 1/3 or 1/4 of the core clock (for 4K LVs, it will always be 1/2 of the core clock). This relationship between the core clock and the GCLKB output is true regardless of whether the PLL is bypassed or not. This clock should not be used externally on the PCB, since all AC timing parameters are specified with regards to the GCLK input clock. It is only provided for test & debug purposes.
GRST2_N	I	Additional reset for production testing. This pin should always be tied high (deasserted).
GBYPASS	I	Controls PLL bypass mode. Typically the PLL is used when operating the LV bus interface in SysAD64 mode, whereas it should most likely not be used when operating in core bond-out mode.
GMULT[1:0]	I	Selects PLL multiplier between externally supplied GCLK and internally generated core clock. It also controls the divider between the internal core clock and the GCLKB output. On the older 4K LVs, the multiplier is fixed to 2x, regardless of these input pins. On newer 4K LVs, and all 4KE/4KS and 5K LVs, the following values on GMULT[1:0] are supported: 00: Reserved 01: 2x 10: 3x 11: 4x
Static configuration pins		
Pin name	**Type**	**Description**

Table 3 Shared Function Pins (Continued)

CBIGEN	I	Endianess. Configures either big-endian or little-endian mode.
CTIMER5	I	If asserted the interrupt signal from the internal timer in the CPU is muxed onto interrupt input 5 internally in the LV. If deasserted, the timer interrupt output signal from the core does not go anywhere in SysAD64 mode (in bond-out mode, it is available on SI_TimerInt).
CSYSAD	I	Selects SysAD64 bus mode (asserted) or core bond-out (deasserted).
CPIPEWR	I	SysAD64: Selects pipelined writes or R4K style writes on SysAD bus. If the chip is being operated in core bond-out mode, the value on this pin is ignored. See the SysAD bus protocol description in a later chapter for details.
C4WBLK	I	SysAD64: External agent supports 4 word (2 dword) block bursts. If the chip is being operated in core bond-out mode, the value on this pin is ignored. This input put is ignored by the 5K LVs, as they will always perform 4 dword bursts. See the SysAD bus protocol description in a later chapter for details.
EJTAG pins		
Pin name	**Type**	**Description**
ETCK	I	Test clock. External 1k pull-up on PCB must be implemented.
ETMS	I	Test mode. External 1k pull-up on PCB must be implemented.
ETDI	I	Test data input. External 1k pull-up on PCB must be implemented.
ETDO	O (3S)	Test data output
ETRST_N	I	Reset TAP controller. External 1k pull-down on PCB must be implemented.
EDINT	I	External debug interrupt. External 1k pull-up on PCB must be implemented.
ERES[11:0]	O	Reserved.
PDtrace pins		
Pin name	**Type**	**Description**
TR_Probe_n	I	Probe present. External pull-up on PCB must be implemented.
TR_TrigIn	I	Extern trigger input. External pull-down on PCB must be implemented.
TR_TrigOut	O	Extern trigger output.
TR_Clk	O	Trace clock.
TR_Data[7:0]	O	Trace data.
TR_DM	O	DebugMode. Is identical to EJ_DebugM, and shares the same physical pin on the LV.

Table 3 Shared Function Pins (Continued)

Test mode pins (implementor use only)		
Pin name	**Type**	**Description**
TSE	I	Scan enable. Must be deasserted (tied low).
TSM	I	Scan mode. Must be deasserted (tied low).
TSI	I	Scan chain data input. Must be deasserted (tied low).
TSO	O	Scan chain data output. Must be left unconnected.
TIN[3:0]	I	Test mode input pins. Must be deasserted (tied low).
TIN_N[3:0]	I	Test mode input pins. Must be deasserted (tied high).
TOUT[3:0]	O	Test mode output pins. Must be left unconnected.
Test mode pins (MIPS use only)		
Pin name	**Type**	**Description**
MBUS[1:0]	I	Bus test modes. Must be deasserted (tied low).
MINP[2:0]	I	Test mode input pins. Must be deasserted (tied low). Since one or more of these pins might become outputs on future devices, a weak pull-down (47k) must be employed.
MINP_N[2:0]	I	Test mode input pins. Must be deasserted (tied high). Since one or more of these pins might become outputs on future devices, a weak pull-up (47k) must be employed.

All EJTAG pins will typically on the PCB be routed to the EJTAG probe connector. In order to insure stable operation when there is no EJTAG probe attached, the above mentioned pull-ups and -downs must be implemented on the PCB. No pullups/downs are present in the I/O buffers on the LV chip.

Similarly, the above mentioned pull-ups and pull-downs on the PDtrace signals must be implemented on the PCB regardless whether the PDtrace probe connector is present or not. The two PDtrace inputs should never be left floating.

2.2 Functional Pin Specification in SysAD64 Mode

Table 4 Multiplexed Pin Functions in SysAD64 Mode

Global system level pins		
Pin name	**Type**	**Description**
GRST_N	I	Reset. The reset pin must be asserted for at least 16 cycles. It may be both asserted and deasserted asynchronously, as the release point is internally synchronized to the core clock. There is no distinction between reset & cold reset, all resets perform a cold reset on the core.
SysAD64 bus pins		
Pin name	**Type**	**Description**
SSYSAD[63:0]	I/O	Multiplexed address/data bus
SSYSCMD[8:0]	I/O	Command/data identifier bus

Table 4 Multiplexed Pin Functions in SysAD64 Mode (Continued)

SSYSADC[7:0]	I/O	Check bus (parity for SSYSAD)
SSYSCMDP	I/O	Check bus (parity for SSYSCMD). Currently unused.
SRDRDY_N	I	Read ready
SWRRDY_N	I	Write ready
SVALIDIN_N	I	SSYSADP, SSYSCMDP, SSYSADCP from external agent valid
SVALIDOUT_N	O	SSYSADP, SSYSCMDP, SSYSADCP from CPU valid
SEXTRQST_N	I	External agent bus request line. Currently unused.
SRELEASE_N	O	Bus is being released to the external agent
Interrupt pins		
Pin name	**Type**	**Description**
IINT_N[5:0]	I	Interrupt inputs. These 6 lines are double synchronized, and then go directly to the 4K/5K core interrupt input ports through an inverter. IINT_N[5] use is determined by the CTIMER5 configuration pin. If CTIMER5 is asserted, IINT_N[5] will be unused.
INMI_N	I	NMI (Non-Maskable interrupt) input. Double synchronized, and then connected to the CPU core NMI input through an inverter. The INMI_N input is edge-triggered on the falling edge. The minimum duration of the negative pulse in order to insure detection is 1.5 core clock periods. If the pulse is shorter than 1.5 periods, detection cannot be guaranteed.
Unused pins		
Pin name	**Type**	**Description**
EB_WData[63:28]	O	
EB_RData[63:0]	I	
EB_WBErr	I	
EB_EWBE	I	
EB_SBlock	I	
SI_Reset	I	
SI_MergeMode[1]	I	
SI_SimpleBE[0]	I	(Previously this pin was named SI_MergeMode[0])
SI_RP	O	
SI_EXL	O	
EJ_PerRst	O	
EJ_PrRst	O	
EJ_SRstE	O	
EJ_DebugM (TR_DM)	O	On LV's supporting PDtrace this pin is named TR_DM and is used as part of the PDtrace pin group (see TR_DM in the previous table). For LV's without PDtrace this pin carries the EJ_DebugM core output (logically identical to TR_DM), which is not really useful in SysAD64 mode.

Table 4 Multiplexed Pin Functions in SysAD64 Mode (Continued)

PM_DCacheHit	O	The performance monitoring pins are directly driven by the 4K or 5K core. They are actually also valid in SysAD64 bus modes. It should be noted however, that they are not synchronized to the bus clock, but rather to the internal core clock, so they might be difficult to sample in PLL mode as the internally generated core clock is not available on a pin. This is why they are placed in the “unused” section of this table.
PM_DCacheMiss	O	
PM_ICacheHit	O	
PM_ICacheMiss	O	
PM_InstnComplete	O	
PM_ITLBHit	O	
PM_ITLBMiss	O	
PM_JTLBHit	O	
PM_JTLBMiss	O	
PM_WTBMerge	O	
PM_WTBNoMerge	O	
PM_DTLBHit	O	
PM_DTLBMiss	O	

When operating in SysAD64 mode, all the unused inputs must be tied either high or low to avoid floating inputs. All unused outputs should be left unconnected (or the output value should be ignored).

2.3 Functional Pin Specification in Core Bond-out Mode

The table in this section is structured somewhat different that the table in the previous section. The first column gives the pin an alternate name, which is related to the function in core bond-out mode, and the "Type" column specifies the I/O type for the signal (and *not* the physical pin type). The "Physical pin name" column shows which physical pin (in most cases a SysAD64 bus pin) is being used for the function. Note that the physical pin type might be a superset of the type specified for the alternate function (typically physically bidirectional pins are being used for either I or O in core bond-out mode).

If the "physical pin name" field is empty, the core bond-out pin has a dedicated pin which is only used in bond-out mode. There are quite a few of these pins, as there are many more active pins in bond-out mode compared to SysAD64 mode, primarily due to the split unidirectional A/D busses.

When the chip is operating with the bus in bond-out mode, all 4K and 5K core signals are directly available on physical pins, with very few exceptions. The signals not available are listed in two tables at the end of this section.

The naming convention with "_N" for negative polarity signals does not apply for all pin names in this table, as the alternate pin names have been directly taken from the port names on the 4K and 5K cores.

Table 5 Multiplexed Pin Functions in Core Bond-out Mode

EC interface pins			
Alternate function	**Type**	**Physical pin name**	**Description**
EB_A[35:2]	O	SSYSAD[35:2]	5K LV: only EB_A[35:3] used
EB_WData[27:0]	O	SSYSAD[63:36]	

Table 5 Multiplexed Pin Functions in Core Bond-out Mode (Continued)

EB_WData[63:28]	O		4K LV: only EB_WData[31:0] used
EB_RData[63:0]	I		4K LV: only EB_RData[31:0] used
EB_BE[7:0]	O	SSYSADC[7:0]	4K LV: only EB_BE[3:0] used
EB_AValid	O	SSYSCMD[8]	
EB_Write	O	SSYSCMD[7]	
EB_Instr	O	SSYSCMD[6]	
EB_Burst	O	SSYSCMD[5]	
EB_BFirst	O	SSYSCMD[4]	
EB_BLast	O	SSYSCMD[3]	
EB_BLen[1:0]	O	SSYSCMD[2:1]	
EB_ARdy	I	SRDRDY_N	
EB_RdVal	I	SWRRDY_N	
EB_WDRdy	I	SVALIDIN_N	
EB_RBErr	I	SEXTRQST_N	
EB_WBErr	I		
EB_WWBE	O	SSYSCMD[0]	
EB_EWBE	I		
EB_SBlock	I		
System Interface pins			
Alternate function	**Type**	**Physical pin name**	**Description**
SI_Int[5:0]	I	IINT_N[5:0]	See the section below for more information on SI_MergeMode[1] and SI_SimpleBE[0].
SI_NMI	I	INMI_N	
SI_ColdReset	I	GRST_N	
SI_Reset	I		
SI_MergeMode[1]	I		
SI_SimpleBE[0]	I		
SI_RP	O		
SI_Sleep	O	SSYSCMDP	
SI_TimerInt	O	SVALIDOUT_N	
SI_ERL	O	SRELEASE_N	
SI_EXL	O		
EJTAG pins			

Table 5 Multiplexed Pin Functions in Core Bond-out Mode (Continued)

Alternate function	Type	Physical pin name	Description
EJ_PerRst	O		
EJ_PrRst	O		
EJ_SRstE	O		
EJ_DebugM (TR_DM)	O		On LV's supporting PDtrace this pin is named TR_DM and is used both as part of the PDtrace pin group (see TR_DM in the shared pin table) and as a core port output (EJ_DebugM), usable in the system logic. For LV's without PDtrace this pin carries the EJ_DebugM core output.
Performance Monitoring pins			
Alternate function	**Type**	**Physical pin name**	**Description**
PM_DCacheHit	O		All these pins are exact copies of ports on the 4K/5K core. The PM_WTBMerge and PM_WTBNoMerge pins are only valid on 4K LVs. On 5K LVs, these pins are reserved for future use. The PM_DTLBHit and PM_DTLBMiss pins are not valid on 4K LVs based on RTL versions prior to 3.0 (no DTLB in these parts). All other 4K LVs as well as all 4KE, 4KS & 5K LVs drive these pins.
PM_DCacheMiss	O		
PM_ICacheHit	O		
PM_ICacheMiss	O		
PM_InstnComplete	O		
PM_ITLBHit	O		
PM_ITLBMiss	O		
PM_JTLBHit	O		
PM_JTLBMiss	O		
PM_WTBMerge	O		
PM_WTBNoMerge	O		
PM_DTLBHit	O		
PM_DTLBMiss	O		
Unused pins			
Alternate function	**Type**	**Physical pin name**	**Description**
N/A	O	SSYSAD[1:0]	

When operating in core bond-out mode, all the unused inputs (there are currently none) must be tied either high or low to avoid floating inputs. All unused outputs should be left unconnected (or the output value should be ignored).

2.3.1 SI_MergeMode, SI_SimpleBE changes

Since the first release of this document and the associated MIPS 4K and 5K cores, some of the cores have been enhanced with two new ports: SI_SimpleBE[1:0]. At the same time, the meaning of the SI_MergeMode[1:0] ports has been

changed. For more detailed information on the actual functionality of these ports, please refer to the relevant "Integrator's guide" for the core in question.

For the new cores that have both SI_MergeMode[1:0] and SI_SimpleBE[1:0], the LV pinout in core bond-out mode has been slightly changed compared to previous versions of this datasheet. The two balls that previously controlled the two SI_MergeMode inputs to the core now control one bit of SI_MergeMode (SI_MergeMode[1]) and one bit of SI_SimpleBE (SI_SimpleBE[0]). This combination has been chosen in order to make the two variants of the LV's as compatible as possible, seen from the outside.

The changes and their effect are described in the two tables below. The first table details which core ports the two LV balls in question are actually routed to inside the various LV types.

The second table describes for each possible value on the two LV balls, how the different LV types will react with respect to write merging and possible byte enable (BE) combinations which can be presented on the EC interface.

Table 6 Routing of LV balls B10:A11 to SI_MergeMode and SI_SimpleBE

Ball name	Previous pin name	Current pin name	4K LV use	4KE/4KS LV use	5Kc LV use RTL ver. 2.2 or earlier	5Kc/f LV use RTL ver. 2.3 or later
B10	SI_MergeMode[1]	SI_MergeMode[1]	SI_MergeMode[1]	SI_MergeMode[1]	Not used	Not used
A11	SI_MergeMode[0]	SI_SimpleBE[0]	SI_MergeMode[0]	SI_SimpleBE[0]	Not used	SI_SimpleBE[0]

Table 7 Meaning of values on LV balls B10:A11

Value on B10:A11	4K LV SI_MergeMode[1:0]	4KE/4KS LV SI_MergeMode[1] : SI_SimpleBE[0]	5Kc LV RTL ver. 2.2 or earlier	5Kc/f LV RTL ver. 2.3 or later
00	No merge Only "natural" MIPS BE combinations	No merge Only "natural" MIPS BE combinations	Value on inputs ignored. Functionality is always: No merge Only "natural" MIPS BE combinations	No merge Only "natural" MIPS BE combinations
01	SysAD compliant merge Only SysAD compliant BE combinations	No merge Only naturally aligned B,H,W BE combinations		No merge Only naturally aligned B,H,W,D BE combinations
10	Full merge All BE combinations possible	Full merge All BE combinations possible		No merge Only "natural" MIPS BE combinations
11	Reserved	Full merge Only naturally aligned B,H,W BE combinations		No merge Only naturally aligned B,H,W,D BE combinations

2.3.2 Unavailable Core Ports in Bond-out Mode

In core bond-out mode, there are a some ports on the core which are not available as pins on the LV. The two tables below show these pins for both the 4K and 5K LVs (there are a few differences).

Table 8 Unavailable 4K Core Ports in Bond-out Mode

Port name	Comment
EJ_ManufID[10:0]	The values hardcoded on these three core inputs are LV specific and determined by the chip manufacturer.
EJ_PartNumber[15:0]	
EJ_Version[3:0]	
EJ_DINTsup	Hardwired to 1
TR_Data[15:8]	Only TR_Data[7:0] is brought out as LV pins (relevant only for LV's with PDtrace support).
CP*	4K: Doesn't have a coprocessor I/F, so this does not apply. 4KE,4KS: None of the coprocessor signals are brought out.
SI_MergeMode[0]	4K: Is available (see previous section). 4KE,4KS: Hardwired to 0
SI_SimpleBE[1]	4K: Port does not exist on the core. 4KE,4KS: Hardwired to 0
SI_Slip	4K,4KE: Port does not exist on the core. 4KS: Hardwired to 0
SI_ClkOut	
Scan related signals	
Memory BIST related signals	

Table 9 Unavailable 5K Core Ports in Bond-out Mode

Port name	Comment
EJ_ManufID[10:0]	The values hardcoded on these four core inputs are LV specific and determined by the chip manufacturer.
EJ_PartNumber[15:0]	
EJ_Version[3:0]	
SI_PRIdOpt[7:0]	
EJ_DINTsup	Hardwired to 1
EB_BusClkActive	Hardwired to 1
CP*	None of the coprocessor signals are brought out.
SI_SimpleBE[1]	Hardwired to 0
SI_ClkOut	
Scan related signals	
Memory BIST related signals	

3 Clocking and Reset

The LV can be operated in two basic modes, SysAD64 with PLL enabled and core bond-out with PLL in bypass mode. Although the PLL bypass and the bus mode are controlled by individual pins, the two remaining options (SysAD64/bypass & bondout/PLL) are only intended for debugging and should not be used.

3.1 SysAD64 with PLL Enabled

In this mode, the LV is being fed with the bus clock on the GCLK pin. This clock is the reference for all the AC specs on the SysAD64 pins.

Internally, the bus clock is being multipled by a factor of 2,3 or 4 to get the core clock which is being supplied to the CPU.

The clock multiplier support in 4K LVs is depending on the RTL version they are built on. Versions built using RTL version 3.2 or earlier supports only the 2x multiplier. Newer versions (RTL version 3.3 and later) support the full range of clock multipliers (2x, 3x, 4x). The RTL version for a specific LV is documented in the “Specification Update” document for that particular silicon. All versions of 4KE and 4KS LVs support all three clock multipliers.

3.1.1 Reset

The GRST_N pin is internally synchronized, so it can be asserted & deasserted asynchronously to the clock. GRST2_N should be deasserted at all times (tied high). All resets are cold resets, it is not possible to perform a warm reset.

The minimum reset pulse width is 16 clock cycles. After power-up, reset should be asserted for at least 100 ms to allow the PLL to stabilize.

3.2 Core Bond-out with PLL Bypassed

In this mode, the clock supplied on the GCLK pin is fed directly to core. The PLL is not used at all, and the setting on the multiplier configuration pins is ignored.

All AC specs in this mode are related to the GCLK clock.

3.2.1 Reset

In core bond-out mode, the reset ports on the CPU core (both cold & warm) are directly controllable from LV pins. No synchronization is performed, so core timing must be insured from the external world.

GRST2_N should always be deasserted.

4 Bus Protocols

As mentioned earlier, one of the key features of the LV is that it supports two bus modes, the native core EC interface mode (core bond-out mode), and the industry-standard SysAD64 bus.

This chapter will describe each of the modes in more detail.

4.1 SysAD64 Bus Mode

The SysAD interface allows the LV core to be connected to an external agent, like e.g. the Galileo GT-64120 system controller, which gives access to SDRAM, PCI interfaces and various peripherals. The LV/SysAD bus controller has the following SysAD64 interface features:

- Supports both R4000 write mode and pipelined write mode
- Master only interface (i.e. external requests are not supported)
- Registers on all SysAD signal pins
- No more than one outstanding command at any time
- Zero waitstates on writes (write pattern “DDDD” only)
- Interfaces to system controllers from Galileo, NEC, IDT and NKK
- Can utilize 4-word block transfers, if supported by external agent (4K LVs only)

SysAD64 is a fully synchronous bus protocol, and all inputs & outputs conceptually go directly to/from flops. However, in reality this is not true since the SysAD bus controller logic is clocked with the same clock as the core, which is a multiple of 2, 3 or 4 of the bus clock (see GMULT[1:0] in Table 12). On the input side, there is a mux on the flop inputs which is controlled such that data is only sampled at the rising edge of the bus clock (every second, third or fourth rising edge of core clock). Note that the core:bus clock multiplier is fixed at 2x on the earlier versions of 4K LVs.

In addition to SysAD64, the LV bus interface logic also supports a "core bond-out" mode, where all relevant core pins are brought out to physical pins. Which bus mode the chip comes up in is selected through a mode pin (CSYSAD). This mode adds an additional level of muxing on all output pins, so in reality they are not truly driven directly by flops in SysAD64 mode.

4.1.1 SysAD Interface Signals

The SysAD system interface pin names are listed in Table 10, and their traditional signal names (using mixed case without the S-prefix and the optional _N suffix) are given in below:

Table 10 SysAD Interface Signals

Signal name	Type	Description
SysAD[63:0]	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and the external agent
SysCmd[8:0]	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and the external agent
SysADC[7:0]	Input/Output	SysAD parity check bus An 8-bit bus containing parity check bits for the SysAD bus during data cycles

Table 10 SysAD Interface Signals

Signal name	Type	Description
SysCmdP	Input/Output	SysCmd parity check - currently unused
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus
ValidIn*	Input	Valid input Signals that the external agent is now driving a valid address or data on the SysAD bus and a valid data identifier on the SysCMD bus
WrRdy*	Input	Write ready Signals that the external agent is ready to accept a processor write request
RdRdy*	Input	Read ready Signals that the external agent is ready to accept a processor read request
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
ExtRqst*	Input	External request - currently unused

Signals marked with an asterisk (like e.g. Release*) are asserted active low. Note that the ExtRqst* (External request) signal known from other CPUs SysAD interfaces are not used, since most external agents do not have it.

4.1.2 SysAD Bus Controller Configuration Signals

Not all external agents support the same SysAD features. In order to let the LV/SysAD bus controller be able to interface to all external agents, the following configuration signals exist:

Table 11 SysAD64 Configuration Signals

Pin name	Type	Description
CPIPEWR	Input	Write mode (for single write transactions): 0: R4000 compatible write mode (with 2 unused cycles after each write) 1: Pipelined write mode (not supported by all EAs)
CMULT[1:0]	Input	4K LVs (older versions): Unused, the core/bus clock ratio is fixed at 2x
		4K LVs (newer versions) and all 4KE, 4KS and 5K LVs: The core/bus clock ratio is configured as follows: 00: reserved 01: 2x 10: 3x 11: 4x

Table 11 SysAD64 Configuration Signals (Continued)

Pin name	Type	Description
C4WBLK	Input	4K LV: 4-word block transactions supported by external agent (2-dword bursts): 0: No, not supported (e.g. NEC VR5064) 1: Yes, supported (e.g. Galileo GT-64120)
		5K LV: N/A since the 5K LVs always use 8-word blocks (4-dword bursts), which all SysAD64 compliant external agents support.

4.1.3 Commands and Data Identifiers

The SysAD[63:0] bus is a multiplexed address/data bus. The LV/SysAD64 bus controller drives the SysAD bus for a single bus cycle, then it either drives write data, or floats the bus in anticipation of returned read data.

The SysCmd[8:0] bus identifies the contents of the SysAD bus during any cycle in which it is valid. The SysCmd bus carries transaction informations like direction (read/write) and size (block of words or byte, halfword, word, etc.), and the status of the data (good/bad/last). The SysCmd bus is driven by the LV/SysAD64 bus controller during address cycles and during write data cycles, and driven by the external agent during read response cycles.

The SysADC[7:0] bus contains parity bits for each of the bytes on the SysAD[63:0] bus. The timing on SysAD, SysADC, SysCmd and SysCmdP busses is identical; i.e. the direction and validity (with respect to ValidOut* and ValidIn*) is the same for all four busses.

4.1.4 SysCmd Bits

The SysCmd bits have the following meanings:

Table 12 SysCmd Bits

SysCmd bit	Function
SysCmd[8]	0 - Transaction info (read/write/size) 1 - Data identifier (good/bad/last)
SysCmd[7]	0 - last data during data cycles. 1 - not last data during data cycles. Must be 0 for address cycles.
SysCmd[6]	0 - read transaction address or response data 1 - write transaction address or write data
SysCmd[5]	0 - data is good 1 - data is erroneous Must be 0 for address cycles.
SysCmd[4]	0 - check the data & check bits during data cycles 1 - do not check the data & check bits during data cycles Must be 1 for address cycles
SysCmd[3:0]	Encoded data transfer size during address cycles, and reserved during data cycles.

4.1.5 SysCmd encodings for the address cycles

The SysCmd encodings for the address cycles (driven by the LV/SysAD bus controller) is given in the table below. Some of the commands listed below cannot be issued by the 4K LVs, because the 4K core is a 32-bit processor, and the

SysAD64 bus is designed for 64-bit CPUs. A “+” in the “4K LV” column indicates that it is a possible command on the 4K LV SysAD64 interface, and an “+” in the 5K LV column indicates the same for 5K LVs.

Table 13 SysCmd Encoding in Address Cycle

SysCmd[8:0] encoding									Command	Description	4K LV	5K LV
8	7	6	5	4	3	2	1	0				
0	0	0	0	1	1	0	0	0	RdByte	Read a single byte	+	+
0	0	0	0	1	1	0	0	1	RdShort	Read halfword (16 bits)	+	+
0	0	0	0	1	1	0	1	0	RdTribyte	Read 3 bytes	+	+
0	0	0	0	1	1	0	1	1	RdWord	Read single word (32 bits)	+	+
0	0	0	0	1	1	1	0	0	Rd5Byte	Read 5 bytes	-	+
0	0	0	0	1	1	1	0	1	Rd6Byte	Read 6 bytes	-	+
0	0	0	0	1	1	1	1	0	Rd7Byte	Read 7 bytes	-	+
0	0	0	0	1	1	1	1	1	RdDWord	Read double-word (64 bits)	-	+
0	0	0	0	1	0	0	0	0	Rd4Words	Read 4 words in a 2 double-word burst	+[a]	-
0	0	0	0	1	0	0	0	1	Rd8Words	Read 8 words in a 4 double-word burst	+[b]	+
0	0	1	0	1	1	0	0	0	WrByte	Write a single byte	+	+
0	0	1	0	1	1	0	0	1	WrShort	Write halfword (16 bits)	+	+
0	0	1	0	1	1	0	1	0	WrTribyte	Write 3 bytes	+	+
0	0	1	0	1	1	0	1	1	WrWord	Write single word (32 bits)	+	+
0	0	1	0	1	1	1	0	0	Wr5Byte	Write 5 bytes	-	+
0	0	1	0	1	1	1	0	1	Wr6Byte	Write 6 bytes		+
0	0	1	0	1	1	1	1	0	Wr7Byte	Write 7 bytes	-	+
0	0	1	0	1	1	1	1	1	WrDWord	Write double-word (64 bits)	+[b]	+
0	0	1	0	1	0	0	0	0	Wr4Words	Write 4 words in a 2 double-word burst	+[a]	-
0	0	1	0	1	0	0	0	1	Wr8Words	Write 8 words in a 4 double-word burst	-	+

a. 4K LV: Only issued if C4WBLK = 1 (i.e. the external agent supports 4-word block transactions)

b. 4K LV: Only issued if C4WBLK = 0 (i.e. the external agent does not support 4-word block accesses)

4.1.6 SysCmd Encodings for the Read Response Data Cycles

The SysCmd encodings for the read response cycles (driven by the external agent) is given in the table below:

Table 14 SysCmd Encoding in Read Cycles

									Command	Description
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**		
1	1	0	E	0	X	X	X	X	RD&Chk	Indicates valid read data and check bits within a burst. E = 0 : Data is good E = 1 : Data is erroneous
1	1	0	E	1	X	X	X	X	RD&NoChk	Indicates valid read data within a burst (not check bits). E = 0 : Data is good E = 1 : Data is erroneous
1	0	0	E	0	X	X	X	X	REOD&Chk	Indicates last valid read data and check bits in a burst. E = 0 : Data is good E = 1 : Data is erroneous
1	0	0	E	1	X	X	X	X	REOD&NoChk	Indicates last valid read data in a burst (not check bits). E = 0 : Data is good E = 1 : Data is erroneous

‘X’ denotes “don’t care”, but must be driven to a valid 0 or 1 by the external agent. If read data is erroneous (E=1), a bus error is signalled to the CPU core. The error-bit will never be set in write data identifiers.

4.1.7 SysCmd Encodings for the Write Data Cycles

The SysCmd encodings for the write data cycles (driven by the bus controller) is given in the table below:

Table 15 SysCmd Encoding for Write Cycles

									Command	Description
8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**		
1	1	1	E	0	X	X	X	X	WD&Chk	Indicates valid write data and check bits within a burst. E = 0 : Data is good E = 1 : Data is erroneous - never used
1	1	1	E	1	X	X	X	X	WD&NoChk	Indicates valid write data within a burst (not check bits). E = 0 : Data is good E = 1 : Data is erroneous - never used
1	0	1	E	0	X	X	X	X	WEOD&Chk	Indicates last valid write data and check bits in a burst. E = 0 : Data is good E = 1 : Data is erroneous - never used
1	0	1	E	1	X	X	X	X	WEOD&NoChk	Indicates last valid write data in a burst (not check bits). E = 0 : Data is good E = 1 : Data is erroneous - never used

‘X’ denotes “don’t care”, but will be driven to 0 by the LV/SysAD bus controller.

4.1.8 Basic SysAD Access Patterns

A number of SysAD access patterns are showed in the following. In these figures, “a<n>” denotes core address number “<n>” and “d<n>” denotes double word data for core address number “<n>”. Note that a clock-to-output delay of zero is shown.

The issue cycle is defined as the cycle when the external agent can accept the address and command issued from the processor. The LV/SysAD bus controller samples RdRdy* to determine the issue cycle for a processor read, and it samples WrRdy* to determine the issue cycle for a processor write. RdRdy*/WrRdy* must be asserted for one clock cycle, two cycles prior to the address cycle of the processor request to define the address cycle as the issue cycle. RdRdy*/WrRdy* does not need to be asserted during the issue cycle. The processor repeats the address cycle (i.e. asserts ValidOut*) until the conditions of a valid issue cycle are met. After the issue cycle, the bus changes direction in case of a read request, or the bus controller puts write data on the bus in case of a write request.

4.1.9 Read Transactions

The system interface supports a maximum data rate of one double-word per cycle. The rate at which data is delivered to the processor is determined by the external agent, which simply controls the pace by asserting ValidIn* when there is read data on the bus. The order in which data is returned in a read request is “subblock ordering”.

Single Reads (5K LV: 1-8 bytes, 4K LV: 1-4 bytes)

The first figure shows back-to-back read transactions with one wait-state. Cycles 3, 6 and 11 are bus-turnaround cycles. Because the RdRdy* signal is deasserted at the end of cycle 5, cycle 7 is not an issue cycle, and the second read command is “stalled”. The command issues in cycle 10 because RdRdy* is sampled asserted in the end of cycle 8.

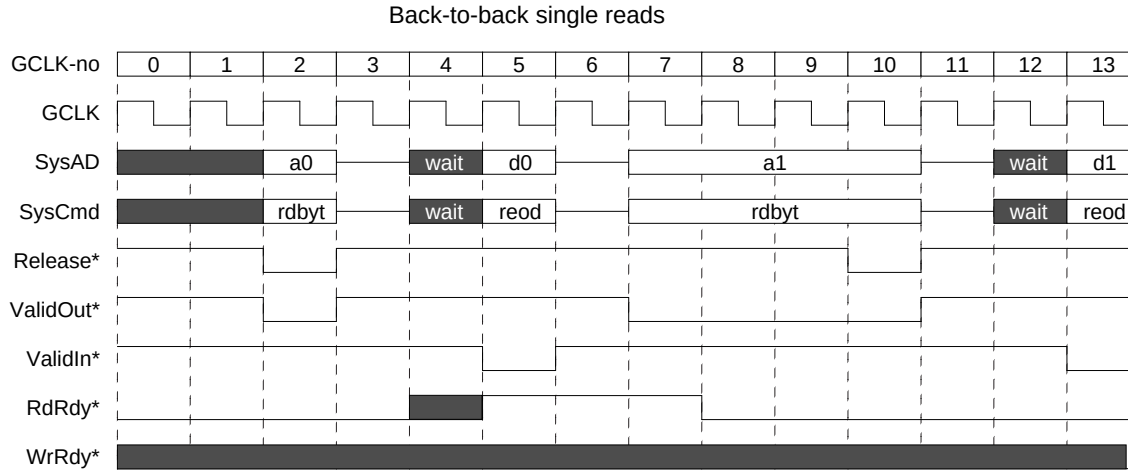

Figure 2 Back-to-back Single Reads

5K LV Core Burst Reads (4 double-words)

The following figure shows back-to-back block read transactions on the 5K LV. 8 words (i.e. 4 double-words) are read in each block transaction:

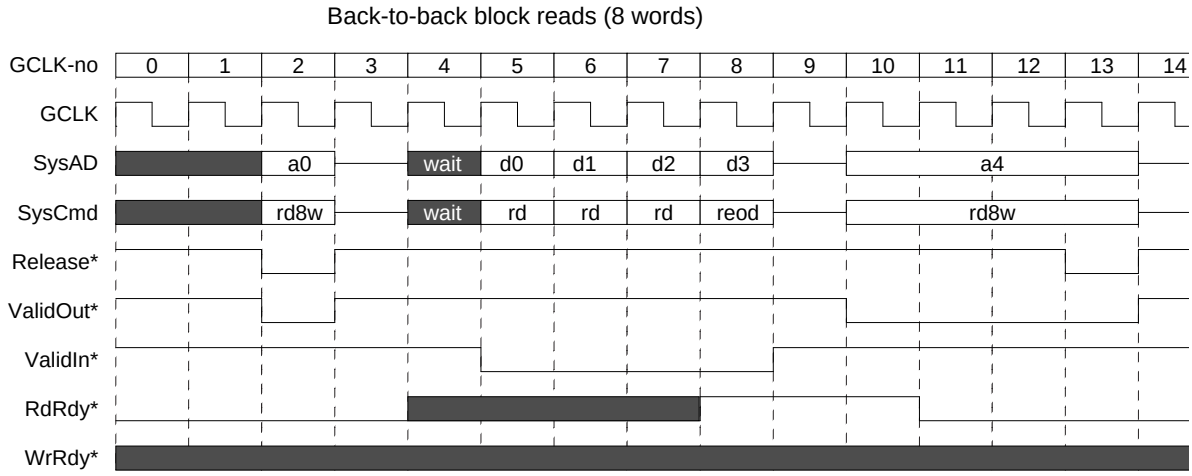

Figure 3 Back-to-back Block Reads

The 4K LVs will perform 8-word block reads in case C4WBLK = 0, when the core issues a burst read of 4 words. The last two read double-words will simply be discarded. If C4WBLK = 1 on the 4K LV, then only two double-words are read in each block, and the external agent must do the bus-turnaround after the second double-word is returned.

4.1.10 Write Transactions

For single writes, the LV/SysAD bus controller supports both pipelined write mode and R4000 compatible write mode. For all writes, the bus controller only supports the “D” write pattern; i.e. there are no wait states between the write data (other than the unused cycles in R4000 mode).

Single Writes (5K LV: 1-8 bytes, 4K LV: 1-4 bytes)

The figure below shows back-to-back single writes in R4000 compatible mode. After each write, there are two unused cycles (ValidOut* is deasserted, but the write data is kept on the bus). This leaves enough time for the external agent to stall the next write command, by deasserting WrRdy* in cycle 5:

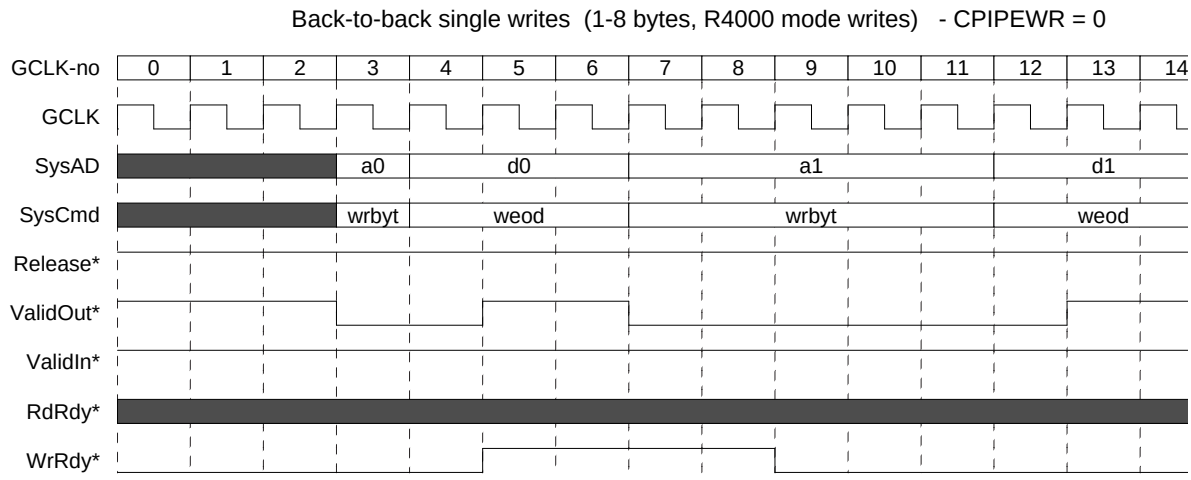

Figure 4 Back-to-back Single Writes

For pipelined writes, there are no unused cycles after the write data, and the external agent must therefore be able to accept one or more writes after it deasserts WrRdy*. This is shown in the figure below:

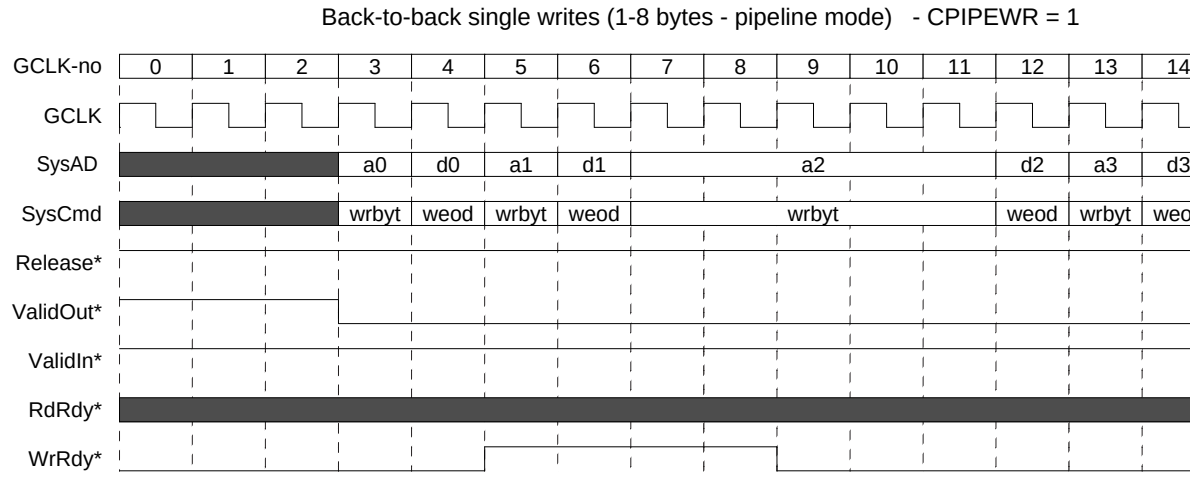

Figure 5 Back-to-back Single Writes

5K LV Core Burst Writes (4 double-words)

The following figure shows back-to-back block write transactions on the 5K LV. 8 words (i.e. 4 double-words) are written in each block transaction:

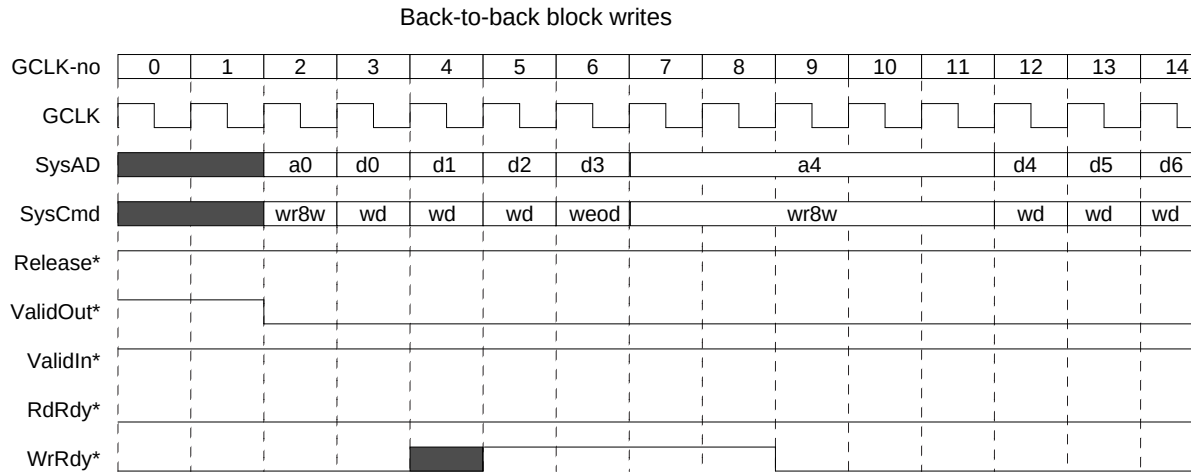

Figure 6 Back-to-back Block Writes

For core burst writes on the 4K LVs, the 4K LV SysAD bus controller will issue 2 doubleword writes in case C4WBLK = 1 (and the access pattern will look just like the one above, except for the “d2” and “d3” data phases, which are removed). Otherwise (C4WBLK = 0), the 4K LV SysAD bus controller will issue two single doubleword writes for each 4-word core burst write.

4.1.11 Low Order SysAD Address Behavior

For SysAD single accesses, the LV SysAD64 interface module converts the byte enable signals on the EC interface to the low order address bits on SysAD. For a 32-bit processor core (4K), the 4 byte enables are converted to the two low

order SysAD address bits, SysAD[1:0], and for a 64-bit (5K) processor core, the 8 byte enables are converted to the three low order SysAD address bits. The conversion also depends on the system endianness, as shown in the tables below:

Table 16 Low Order SysAD Address Generation from 32-bit EC Interface

EB_A[2]	EB_BE[3:0]	SysAD[2:0] in address phase Big endian (SI_Endian = 1)	SysAD[2:0] in address phase Little endian (SI_Endian = 0)
0	1000	0	3
0	0100	1	2
0	0010	2	1
0	0001	3	0
0	1100	0	2
0	0011	2	0
0	1110	0	1
0	0111	1	0
0	1111	0	0
1	1000	4	7
1	0100	5	6
1	0010	6	5
1	0001	7	4
1	1100	4	6
1	0011	6	4
1	1110	4	5
1	0111	5	4
1	1111	4	4

Table 17 Low Order SysAD Address Generation from 64-bit EC Interface

EB_BE[7:0]	SysAD[2:0] in address phase Big endian (SI_Endian = 1)	SysAD[2:0] in address phase Little endian (SI_Endian = 0)
10000000	0	7
01000000	1	6
00100000	2	5
00010000	3	4
00001000	4	3
00000100	5	2
00000010	6	1
00000001	7	0
11000000	0	6

Table 17 Low Order SysAD Address Generation from 64-bit EC Interface

EB_BE[7:0]	SysAD[2:0] in address phase Big endian (SI_Endian = 1)	SysAD[2:0] in address phase Little endian (SI_Endian = 0)
00110000	2	4
00001100	4	2
00000011	6	0
11100000	0	5
01110000	1	4
00001110	4	1
00000111	5	0
11110000	0	4
00001111	4	0
11111000	0	3
00011111	3	0
11111100	0	2
00111111	2	0
11111110	0	1
01111111	1	0
11111111	0	0

The tables above are also valid if the processor core runs user mode code in reverse endian mode. However, in reverse endian mode a 4K LV and a 5K LV will not present the same addresses on the SysAD interface when running the same code. The following short example illustrates why there is a difference here:

Assume a big-endian system (i.e. SI_Endian=1). Assume that a user mode program performs a byte access on virtual address 1. On a 4K core, EB_BE[3:0] will then equal 0010 (because of reverse endian), and EB_A[2] will be 0. This will give SysAD[2:0] = 2 since the system endianness is “big”. But on a 5K core, EB_BE[7:0] will be 00000010 (because of reverse endian), which corresponds to SysAD[2:0] = 6.

This difference in SysAD address behavior between 4K and 5K lead vehicles must be kept in mind, when designing systems that utilize reverse endian mode.

4.2 Core Bond-out Mode

The core bond-out bus mode will basically make all pins on the 4K/5K microprocessor core, including the entire EC interface, available on the physical LV pins. The intention of this mode is to allow board-level prototyping of SOC applications, using exactly the same bus protocol between the processor and the rest of system which would exist in a final ASIC.

There are a few core pins not being brought out in this mode, e.g. the core pins related to production testing (scan etc.). For some of the newer core types, interfaces like UDI and CoProcessor interfaces are also not brought out due to pin limitations.

The EC interface itself and the protocol will not be described in more detail here, please see the appropriate core documentation for additional information. Normally the bus protocol information for a specific core is located in the "Integrator’s Guide" covering that particular core family.

An important note is however that the 4K cores employ the 32-bit version of the EC interface, whereas 5K cores use the 64-bit version. The 64 bit version is a superset of the 32 bit version, the only difference being the bus width.

The LV pinout is supporting the full 64 bit version of the EC interface in bond-out mode, and this means there are a number of unused pins on the 4K LV. However, these input pins should not be left floating on the PCB, they should be tied to either VSS or VDD.

4.3 General PCB Design Rules

Since the two bus modes supported by the LV do not use an identical set of pins, there are some unused inputs & outputs pins in both modes. For both modes, all the unused inputs on the LV should be tied to either VSS or VCC on the PCB.

5 AC, DC Specifications

This chapter lists the general AC & DC requirements on a per-pin basis. Please observe that all the timing presented in this chapter is a “target specification”, which all LV implementations will do their best to achieve. For actual LV silicon specifications, please refer to the “Specification Update” documents, which are issued for each LV implementation. There is more information on this (including MD document numbers for the specification updates) in the chapter covering implementation specific data.

The information has been split into three tables: one covering shared pins with identical functions in SysAD64 and bond-out mode, and two tables covering multiplexed pins with different function in the two modes. Note that the AC spec for a multiplexed dual-function pin is typically not the same for both bus modes. The mode specific tables do not include entries for pins which are unused in that particular mode.

All I/O levels are 3.3V with TTL thresholds. The I/O buffers are capable of both driving (output buffers only) and tolerating (input buffers only) 3.3V on the pin. There is no 5V drive capability or input tolerance on any pin. There are no internal pull-ups/pull-downs in the I/O buffers on the LV.

The I/O buffers are further characterized in the table through a DC-drive specification. This specifies how much DC current the buffer is able to source or sink without violating the thresholds.

The environmental conditions for which the specified timing parameters are guaranteed, are ambient temperatures from 0-70 degrees celcius (no air flow), and a supply voltage range within +/- 5% from the nominal value.

5.1 AC/DC Specifications for Pins with Identical Function in Both Modes

Table 18 AC/DC Pin Specs for Shared Function Pins

Pin name	Type	DC drive [mA]	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
GCLK	I							
GCLKB	O	"4"	25	CoreCLK[a]	-2	0		
GRST2_N	I			DC				
GBYPASS	I			DC				
GMULT[1:0]	I			DC				
CBIGEN	I			DC				
CTIMER5	I			DC				
CSYSAD	I			DC				
CPIPEWR	I			DC				
C4WBLK	I			DC				
ETCK	I							
ETMS	I			DC				
ETDI	I			ETCK			4	1

Table 18 AC/DC Pin Specs for Shared Function Pins (Continued)

Pin name	Type	DC drive [mA]	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
ETDO	O (3S)	"8"	50	ETCK[b]	2	5.2		
ETRST_N	I			DC				
EDINT	I			ASYNC				
ERES[11:0]	O	"8"	50					
TR_Probe_n	I			DC				
TR_TrigIn	I			ASYNC				
TR_TrigOut	O	"6"		ASYNC				
TR_Clk	O	"6"						
TR_Data[7:0]	O	"6"		TR_Clk[c]	-1	1		
TR_DM	O	"6"		ASYNC				
TSE	I			DC				
TSM	I			DC				
TSI	I			DC				
TSO	O	"4"	25					
TIN[3:0]	I			DC				
TIN_N[3:0]	I			DC				
TOUT[3:0]	O	"4"	25					
MBUS	I			DC				
MINP[2:0]	I			DC				
MINP_N[2:0]	I			DC				

a. The GCLKB output timing is specified relative to the internal core clock at the flip-flops.

b. The ETDO output timing is specified relative to the negative edge of ETCK.

c. The TR_Data is DDR data output with regards to TR_Clk. See the relevant PDtrace specification for details. The timing specification is the maximum jitter of the TR_Data output edges wrt. the TR_Clk edges (both positive and the "ideally" placed negative edge).

All configuration input pins must be held static from at least 16 cycles before reset is released to eternity (or next reset period). If any of these pins change value during the normal operation of the chip, the results are unpredictable. They should only be changed while GRST_N is asserted.

The timing specified for GCLKB is relative to the internal clock of the chip. This output should not be used, it is for debugging purposes only.

The EJTAG clock input (ETCK) must comply with the following specification:

Table 19 ETCK Timing Specifications

Description	Min	Max
ETCK frequency	0 MHz	40 MHz
ETCK high time	10 ns	
ETCK low time	10 ns	

ETDO is referenced to the negative edge of ETCK (LV clocks data out on falling edge, probe samples on rising edge). The EDINT input is double synchronized in the CPU core, so this input may be driven asynchronously.

5.2 AC/DC Specifications for Multiplexed Pins in SysAD64 Mode

All the references to GCLK in SysAD64 mode are specified with the PLL enabled. The SysAD64 is a fully registered and synchronous bus protocol, which makes the AC timing specification for these pins very straightforward. This is the reason why there are no AC timing diagrams in this document.

The frequency range supported by any LV implementation in SysAD64 mode (PLL enabled) is implementation specific. The minimum frequency is typically due to PLL restrictions, whereas the maximum is limited by the design and the technology used. However, there are some core clock frequency ranges that are targeted to work with any LV as listed in the table below.

Table 20 Clock Specifications for SysAD64 Mode

Description	Min	Max
GCLK duty cycle	40/60	60/40
4K LV Core clock frequency target range	100 MHz	120 MHz
GCLK frequency target range (2x multiplier)	50 MHz	60 MHz
GCLK frequency target range (3x multiplier)	33.3 MHz	40 MHz
GCLK frequency target range (4x multiplier)	25 MHz	30 MHz
5K LV Core clock frequency target range	150 MHz	150 MHz
GCLK frequency target range (2x multiplier)	75 MHz	75 MHz
GCLK frequency target range (3x multiplier)	50 MHz	50 MHz
GCLK frequency target range (4x multiplier)	37.5 MHz	37.5 MHz

Table 21 AC/DC Pin Specifications for SysAD64 Mode

Pin name	Type	DC drive [mA]	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
GRST_N	I			ASYNC				

Table 21 AC/DC Pin Specifications for SysAD64 Mode

Pin name	Type	DC drive [mA]	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
SSYSAD[63:0]	I/O	"4"	25	GCLK	2	5	2	0
SSYSCMD[8:0]	I/O	"4"	25	GCLK	2	5	2	0
SSYSADC[7:0]	I/O	"4"	25	GCLK	2	5	2	0
SSYSCMDP	I/O	"4"	25	GCLK	2	5	2	0
SRDRDY_N	I			GCLK			2	0
SWRRDY_N	I			GCLK			2	0
SVALIDIN_N	I			GCLK			2	0
SVALIDOUT_N	O	"4"	25	GCLK	2	5		
SEXTRQST_N	I			GCLK			2	0
SRELEASE_N	O	"4"	25	GCLK	2	5		
IINT_N[5:0]	I			ASYNC				
INMI_N	I			ASYNC				

All 7 interrupt lines (IINT_N and INMI_N) are internally double synchronized, so these lines may be asserted and deasserted asynchronously.

The INMI_N input is asynchronous, but in order to guarantee that the negative edge is detected, the minimum negative pulse width is 1.5 core clock periods.

The minimum Clock-to-output time specified (typically 2 ns) will be satisfied for all pins, even if the load is reduced from the value in the table down to 10 pF.

5.3 AC/DC Specifications for Multiplexed Pins in Core Bond-out Mode

All signals are referenced to GCLK, but with the PLL disabled (running in bypass mode).

Again, the frequency range supported in bond-out mode is LV implementation specific, but the table below lists the frequency ranges and clock specs targetted to work with any LV.

Table 22 Clock Specifications for Core Bond-out Mode

Description	Min	Max
GCLK duty cycle	40/60	60/40
4K LV Core clock frequency target range	0 MHz	75 MHz

Table 22 Clock Specifications for Core Bond-out Mode

Description	Min	Max
5K LV Core clock frequency target range	0 MHz	75 MHz

Table 23 AC/DC Pin Specifications for Core Bond-out Mode

Pin name[a]	Type	DC drive [mA]	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
EB_A[35:2]	O	"4"	25	GCLK	3	10		
EB_WData[63:0]	O	"4"	25	GCLK	3	10		
EB_RData[63:0]	I			GCLK			6	0
EB_BE[7:0]	O	"4"	25	GCLK	3	10		
EB_AValid	O	"4"	25	GCLK	3	10		
EB_Write	O	"4"	25	GCLK	3	10		
EB_Instr	O	"4"	25	GCLK	3	10		
EB_Burst	O	"4"	25	GCLK	3	10		
EB_BFirst	O	"4"	25	GCLK	3	10		
EB_BLast	O	"4"	25	GCLK	3	10		
EB_BLen[1:0]	O	"4"	25	GCLK	3	10		
EB_ARdy	I			GCLK			6	0
EB_RdVal	I			GCLK			6	0
EB_WDRdy	I			GCLK			6	0
EB_RBErr	I			GCLK			6	0
EB_WBErr	I			GCLK			6	0
EB_WWBE	O	"4"	25	GCLK	3	10		
EB_EWBE	I			GCLK			6	0
EB_SBlock	I			GCLK			6	0
SI_Int[5:0]	I			GCLK			6	0
SI_NMI	I			GCLK			6	0
SI_ColdReset	I			GCLK			6	0
SI_Reset	I			GCLK			6	0
SI_MergeMode[1]	I			GCLK			6	0
SI_SimpleBE[0]	I			GCLK			6	0
SI_RP	O	“4”	25	GCLK	3	10		

Table 23 AC/DC Pin Specifications for Core Bond-out Mode (Continued)

Pin name[a]	Type	DC drive [mA]	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
SI_Sleep	O	“4”	25	GCLK	3	10		
SI_TimerInt	O	"4"	25	GCLK	3	10		
SI_ERL	O	"4"	25	GCLK	3	10		
SI_EXL	O	"4"	25	GCLK	3	10		
EJ_PerRst	O	"4"	25	GCLK	3	10		
EJ_PrRst	O	"4"	25	GCLK	3	10		
EJ_SRstE	O	"4"	25	GCLK	3	10		
EJ_DebugM (TR_DM)	O	"4"	25	GCLK	3	10		
PM_DCacheHit	O	"4"	25	GCLK	3	10		
PM_DCacheMiss	O	"4"	25	GCLK	3	10		
PM_ICacheHit	O	"4"	25	GCLK	3	10		
PM_ICacheMiss	O	"4"	25	GCLK	3	10		
PM_InstnComplete	O	"4"	25	GCLK	3	10		
PM_ITLBHit	O	"4"	25	GCLK	3	10		
PM_ITLBMiss	O	"4"	25	GCLK	3	10		
PM_JTLBHit	O	"4"	25	GCLK	3	10		
PM_JTLBMiss	O	"4"	25	GCLK	3	10		
PM_WTBMerge	O	"4"	25	GCLK	3	10		
PM_WTBNoMerge	O	"4"	25	GCLK	3	10		
PM_DTLBHit	O	"4"	25	GCLK	3	10		
PM_DTLBMiss	O	"4"	25	GCLK	3	10		

a. The pins names listed in this table are not physical pin names. See Table 5 for a mapping between the core bond-out mode pins and the physical pin names used on the device.

The minimum Clock-to-output time specified (typically 3ns) will be satisfied, even if the load is reduced from the value in the table down to 10 pF.

5.4 Power Supplies

The chip power supplies has been split into three separate supplies:

- I/O power supply
- Core power supply

- PLL power supply (quiet Vss, Vdd)

The different implementations of the LV have different supplies depending on the technology used. The chip specific supply voltages are listed in the next chapter.

6 Implementation Specific Data

Even though it is the goal to keep the various implementations of the 4K and 5K LVs as identical as possible, they usually differ slightly due to constraints of the underlying technology.

For detailed information on silicon specific data for each LV, a “Specification Update” document is issued for each. These documents are the definitive source of information regarding a specific LV implementation. The information in this chapter is an extract of the information in these documents, presented in a way that makes it easy to distinguish between the top-level differences amongst the LVs. This is particular useful if you are trying to make a design that will be able to work with several different LV’s.

6.1 Identification

The table below lists and identifies all the 4K & 5K LVs that exist as of today. The table is constantly updated as new LVs are being manufactured.

Table 24 LV Identification

Internal ID	Manufacturer	LV type	ID on chip	MD Document number for “Specification Update”
1	Texas Inst. (TI)	4Kc	F731940	MD00004
2	Chartered (CSM)	4Kc/m	J25C1[a]	MD00033
3	Lightspeed (LSS)	5Kc/m	LJA0004	MD00079
4	Texas Inst. (TI)	5Kc/m	F741763	MD00140

a. The actual chip marking is J025C1, typically followed by one or more letters indicating production batch.

The internal ID number in the first column is used throughout this chapter to uniquely identify the LV in the subsequent tables. This avoids having detailed identification information copied throughout all tables in this chapter. The “Specification Update” document associated with each LV is also named in the table.

6.2 Cache Size

As mentioned earlier, some of the 5K LVs have not been implemented with the maximum cache size as specified in this document, due to limitations of the available RAM blocks.

All of the 4K LVs are not mentioned in this table, as they all implement the cache size specified in this document.

Table 25 5K LV Cache Sizes

Internal ID	Cache set size	Associativity (I/D)	Total cache size (I/D)
3	4 kByte	2I, 2D	8 kByte, 8 kByte
4	4 kByte	4I, 4D	16 kByte, 16 kByte

6.3 Supply Voltages

All the different LVs use different supply voltages depending on the technology used. As mentioned earlier, the power supply is split into three separate supplies:

- I/O power supply
- Core power supply
- PLL power supply (quiet Vss, Vdd)

The table below shows the required voltages for each LV implementation.

Table 26 LV Supply Voltages

Internal ID	VDD (I/O buffers)	CVDD (Core)	VDDA (PLL supply)
1	3.3V	1.8V	3.3V
2	3.3V	2.5V	2.5V
3	3.3V	2.5V	2.5V
4	3.3V	1.8V	N/A[a]

a. This chip uses the CVDD to supply the PLL.

All voltages shown above are nominal values. Unless otherwise noted, all power supplies are +/- 5%.

All LV implementations allow the three power supplies to come up in random order at power-on. Same rule applies for power-off scenarios.

6.4 PLL Connections

There are 6 balls reserved for the analog connections to the PLL (quiet supplies, optional loop filter etc.). The connections to these 6 balls are different depending on the actual implementation of the LV.

The pinout in this datasheet (next chapter) describes the “default” PLL pinout, but some of the LVs have different connections on these 6 balls. The connections for all of the LVs are described in the following table.

Table 27 PLL Pinout

Internal ID	B13	D13	A13	C14	B12	C13
1	NC	NC	VSSA	LF	VDDA	NC
2	NC	NC	VSSA	NC	VDDA	NC
3	NC	NC	VSSA	NC	VDDA	NC
4	NC	NC	NC	NC	NC	NC

Note that in some cases, the devices actually drive the NC pins (see the silicon specification update documents for details). These pins must therefore truly be left unconnected.

LF in the table above is the loop filter connection for the PLL. The specifics are described in the next section.

6.5 PLL Loop Filter Types, Component Values and Frequency Range

Between the various LV implementations, there is also a difference in the loop filter construction. Some use internal loop filters, and the LF pin does not exist. The rest use external loop filters, but with varying design and component values. The table below shows the required loop filter for each chip.

Table 28 PLL Loop Filter Types, Component Values and Frequency Range

Internal ID	Loop filter type	Value of R1	Value of C1	Value of C2	Minimum PLL freq	Maximum PLL freq
1	Type 1	62 ohm	16 nF	300 pF	50 MHz	210 MHz
2	Internal	N/A	N/A	N/A	N/A	N/A
3	Internal	N/A	N/A	N/A	N/A	N/A
4	Internal	N/A	N/A	N/A	N/A	N/A

Unless otherwise noted in the table, the components should be +/- 5% or better.

The PLL frequency range shown in the table above is the core clock frequency range supported. The input frequency depends on the multiplication factor being used.

Currently, only one type of loop filter is employed:

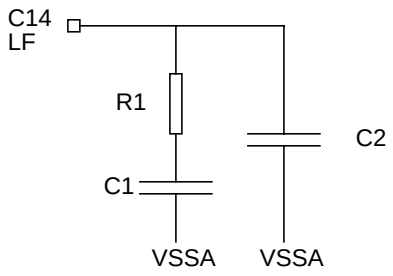

Figure 7 Loop Filter - Type 1

For type 1 loop filters, it is the R1,C1 which are the critical components. These two components must have the shortest possible trace lengths on the PCB connecting to the LV. C2 is also critical, but not as much as R1,C1.

7 Package and Pinout

The LV package is a standard Jedec 388 ball BGA, with 35x35 mm body and 1.27 mm ball pitch (Jedec code MO-151). This package has 16 pre-allocated Vdd balls, and 32 pre-allocated Vss balls (304 I/O balls available). There are also 36 additional Vss balls in the center of the package. The pre-allocated Vdd & Vss balls are used to supply the I/O buffers. The core Vdd supply and the quiet PLL supplies are fed in through "normal" I/O signal balls.

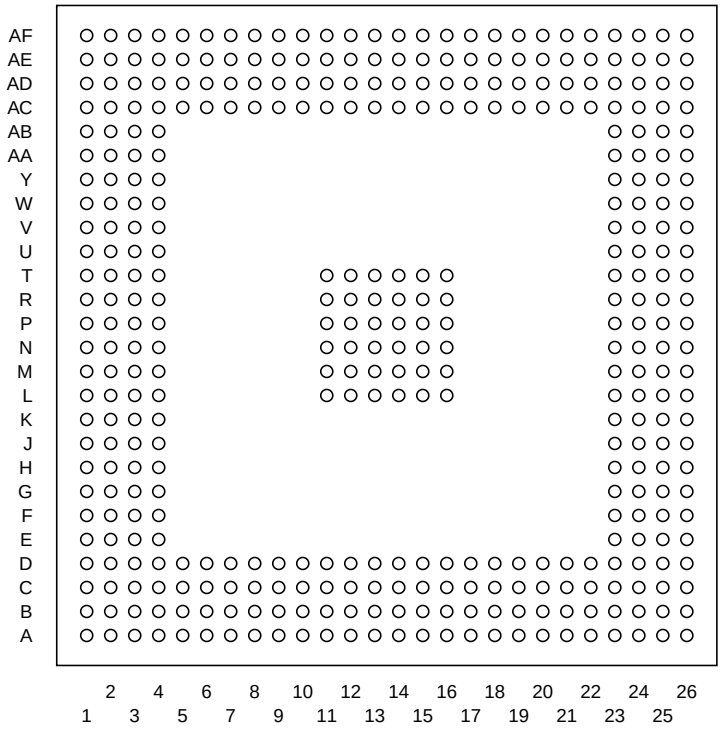

Figure 8 Package Drawing (bottom view)

Table 29 Ball Assignments (pin order)

C4WBLK	AF6	EDINT	C16	SSYSADC[7]	E24
CBIGEN	R1	EJ_DEBUGM (TR_DM)	D2	SSYSCMDP	AF23
CPIPEWR	AE6	EJ_PERRST	E3	SSYSCMD[0]	D18
CSYSAD	AB2	EJ_PRRST	G4	SSYSCMD[1]	C20
CTIMER5	AC1	EJ_SRSTE	F3	SSYSCMD[2]	C21
CVDD	A12	ERES[0]	C9	SSYSCMD[3]	D20
CVDD	A4	ERES[1]	D8	SSYSCMD[4]	B21
CVDD	AE11	ETCK	D1	SSYSCMD[5]	C22
CVDD	AE13	ETDI	G2	SSYSCMD[6]	D22
CVDD	AE15	ETDO	F1	SSYSCMD[7]	B22
CVDD	AE19	ETMS	F2	SSYSCMD[8]	C23
CVDD	AE7	ETRST_N	C1	SVALIDIN_N	B9

Table 29 Ball Assignments (pin order) (Continued)

CVDD	B15	GBYPASS	A14	SVALIDOUT_N	C18
CVDD	B19	GCLK	A15	SWRRDY_N	A21
CVDD	B7	GCLKB	B14	TIN[0]	B6
CVDD	C15	GMULT[0]	A22	TIN[1]	A6
CVDD	E2	GMULT[1]	A23	TIN[2]	B5
CVDD	E25	GRST2_N	A17	TIN[3]	A5
CVDD	G3	GRST_N	D15	TIN_N[0]	A9
CVDD	J24	IINT_N[0]	J2	TIN_N[1]	B8
CVDD	L3	IINT_N[1]	K1	TIN_N[2]	A8
CVDD	N24	IINT_N[2]	L2	TIN_N[3]	A7
CVDD	R3	IINT_N[3]	L1	TOUT[0]	G1
CVDD	U24	IINT_N[4]	M2	TOUT[1]	H2
CVDD	V1	IINT_N[5]	M1	TOUT[2]	H1
CVDD	W3	INMI_N	K2	TOUT[3]	J1
CVDD	Y24	LF	C14	TR_CLK	C4
EB_EWBE	A16	MBUS[0]	AA1	TR_DATA[0]	C8
EB_RDATA[0]	AF2	MBUS[1]	AB1	TR_DATA[1]	D7
EB_RDATA[1]	AF3	MINP[0]	W1	TR_DATA[2]	C7
EB_RDATA[2]	AF4	MINP[1]	Y2	TR_DATA[3]	C6
EB_RDATA[3]	AE5	MINP[2]	Y1	TR_DATA[4]	B4
EB_RDATA[4]	AF5	MINP_N[0]	R2	TR_DATA[5]	D5
EB_RDATA[5]	AF7	MINP_N[1]	U2	TR_DATA[6]	C5
EB_RDATA[6]	AE8	MINP_N[2]	U1	TR_DATA[7]	B3
EB_RDATA[7]	AF8	PLL_NC[0]	C13	TR_PROBE_N	V2
EB_RDATA[8]	AE9	PLL_NC[1]	D13	TR_TRIGIN	AA2
EB_RDATA[9]	AF9	PLL_NC[2]	B13	TR_TRIGOUT	A3
EB_RDATA[10]	AE10	PM_DCACHEHIT	D17	TSE	P1
EB_RDATA[11]	AF10	PM_DCACHEMISS	C17	TSI	N2
EB_RDATA[12]	AF11	PM_DTLBHIT	C2	TSM	N1
EB_RDATA[13]	AE12	PM_DTLBMISS	B1	TSO	E1
EB_RDATA[14]	AF12	PM_ICACHEHIT	A20	VDD	AA23
EB_RDATA[15]	AF13	PM_ICACHEMISS	B20	VDD	AA4
EB_RDATA[16]	AE14	PM_INSTNCOMPLETE	A19	VDD	AC11
EB_RDATA[17]	AF14	PM_ITLBHIT	B11	VDD	AC16

Table 29 Ball Assignments (pin order) (Continued)

EB_RDATA[18]	AF15	PM_ITLBMISS	C12	VDD	AC21
EB_RDATA[19]	AE16	PM_JTLBHIT	D12	VDD	AC6
EB_RDATA[20]	AF16	PM_JTLBMISS	C11	VDD	D11
EB_RDATA[21]	AE17	PM_WTBMERGE	D10	VDD	D16
EB_RDATA[22]	AF17	PM_WTBNOMERGE	C10	VDD	D21
EB_RDATA[23]	AE18	SEXTRQST_N	B17	VDD	D6
EB_RDATA[24]	AF18	SI_EXL	E4	VDD	F23
EB_RDATA[25]	AF19	SI_MERGEMODE[1]	B10	VDD	F4
EB_RDATA[26]	AE20	SI_RESET	A10	VDD	L23
EB_RDATA[27]	AF20	SI_RP	D3	VDD	L4
EB_RDATA[28]	AE21	SI_SIMPLEBE[0]	A11	VDD	T23
EB_RDATA[29]	AF21	SRDRDY_N	B18	VDD	T4
EB_RDATA[30]	AE22	SRELEASE_N	C19	VDDA	B12
EB_RDATA[31]	AF22	SSYSAD[0]	D26	VSS	A1
EB_RDATA[32]	AC26	SSYSAD[1]	E23	VSS	A2
EB_RDATA[33]	AB25	SSYSAD[2]	D25	VSS	A26
EB_RDATA[34]	AB26	SSYSAD[3]	F24	VSS	AC13
EB_RDATA[35]	AA25	SSYSAD[4]	G24	VSS	AC18
EB_RDATA[36]	AA26	SSYSAD[5]	G23	VSS	AC23
EB_RDATA[37]	Y25	SSYSAD[6]	H24	VSS	AC4
EB_RDATA[38]	Y26	SSYSAD[7]	G26	VSS	AC8
EB_RDATA[39]	W25	SSYSAD[8]	H23	VSS	AD24
EB_RDATA[40]	W26	SSYSAD[9]	G25	VSS	AD3
EB_RDATA[41]	V25	SSYSAD[10]	H26	VSS	AE1
EB_RDATA[42]	V26	SSYSAD[11]	H25	VSS	AE2
EB_RDATA[43]	U25	SSYSAD[12]	K24	VSS	AE25
EB_RDATA[44]	U26	SSYSAD[13]	K23	VSS	AF1
EB_RDATA[45]	T25	SSYSAD[14]	L24	VSS	AF25
EB_RDATA[46]	T26	SSYSAD[15]	M23	VSS	AF26
EB_RDATA[47]	R25	SSYSAD[16]	M24	VSS	B2
EB_RDATA[48]	R26	SSYSAD[17]	P24	VSS	B25
EB_RDATA[49]	P25	SSYSAD[18]	N23	VSS	B26
EB_RDATA[50]	P26	SSYSAD[19]	R24	VSS	C24
EB_RDATA[51]	N25	SSYSAD[20]	R23	VSS	C3

Table 29 Ball Assignments (pin order) (Continued)

EB_RDATA[52]	N26	SSYSAD[21]	T24	VSS	D14
EB_RDATA[53]	M25	SSYSAD[22]	U23	VSS	D19
EB_RDATA[54]	M26	SSYSAD[23]	V24	VSS	D23
EB_RDATA[55]	L25	SSYSAD[24]	W24	VSS	D4
EB_RDATA[56]	L26	SSYSAD[25]	V23	VSS	D9
EB_RDATA[57]	K25	SSYSAD[26]	AA24	VSS	H4
EB_RDATA[58]	K26	SSYSAD[27]	Y23	VSS	J23
EB_RDATA[59]	J25	SSYSAD[28]	AB24	VSS	L11
EB_RDATA[60]	J26	SSYSAD[29]	AB23	VSS	L12
EB_RDATA[61]	F25	SSYSAD[30]	AC24	VSS	L13
EB_RDATA[62]	F26	SSYSAD[31]	AC25	VSS	L14
EB_RDATA[63]	E26	SSYSAD[32]	AD26	VSS	L15
EB_SBLOCK	A18	SSYSAD[33]	AD25	VSS	L16
EB_WBERR	B16	SSYSAD[34]	AE26	VSS	M11
EB_WDATA[28]	AD6	SSYSAD[35]	AF24	VSS	M12
EB_WDATA[29]	AC7	SSYSAD[36]	AD23	VSS	M13
EB_WDATA[30]	AD5	SSYSAD[37]	AE24	VSS	M14
EB_WDATA[31]	AC5	SSYSAD[38]	AD22	VSS	M15
EB_WDATA[32]	AD4	SSYSAD[39]	AC22	VSS	M16
EB_WDATA[33]	AE4	SSYSAD[40]	AE23	VSS	N11
EB_WDATA[34]	AE3	SSYSAD[41]	AD21	VSS	N12
EB_WDATA[35]	AD1	SSYSAD[42]	AD20	VSS	N13
EB_WDATA[36]	AC3	SSYSAD[43]	AC20	VSS	N14
EB_WDATA[37]	AD2	SSYSAD[44]	AD19	VSS	N15
EB_WDATA[38]	AB3	SSYSAD[45]	AC19	VSS	N16
EB_WDATA[39]	AB4	SSYSAD[46]	AD18	VSS	N4
EB_WDATA[40]	AC2	SSYSAD[47]	AD17	VSS	P11
EB_WDATA[41]	AA3	SSYSAD[48]	AC17	VSS	P12
EB_WDATA[42]	Y3	SSYSAD[49]	AD16	VSS	P13
EB_WDATA[43]	Y4	SSYSAD[50]	AC15	VSS	P14
EB_WDATA[44]	W4	SSYSAD[51]	AD15	VSS	P15
EB_WDATA[45]	V3	SSYSAD[52]	AD14	VSS	P16
EB_WDATA[46]	W2	SSYSAD[53]	AD13	VSS	P23
EB_WDATA[47]	U3	SSYSAD[54]	AC14	VSS	R11

Table 29 Ball Assignments (pin order) (Continued)

EB_WDATA[48]	U4	SSYSAD[55]	AD12	VSS	R12
EB_WDATA[49]	T3	SSYSAD[56]	AC12	VSS	R13
EB_WDATA[50]	R4	SSYSAD[57]	AD11	VSS	R14
EB_WDATA[51]	T1	SSYSAD[58]	AD10	VSS	R15
EB_WDATA[52]	T2	SSYSAD[59]	AC10	VSS	R16
EB_WDATA[53]	P3	SSYSAD[60]	AD9	VSS	T11
EB_WDATA[54]	N3	SSYSAD[61]	AD8	VSS	T12
EB_WDATA[55]	P4	SSYSAD[62]	AC9	VSS	T13
EB_WDATA[56]	P2	SSYSAD[63]	AD7	VSS	T14
EB_WDATA[57]	M3	SSYSADC[0]	B23	VSS	T15
EB_WDATA[58]	M4	SSYSADC[1]	A24	VSS	T16
EB_WDATA[59]	K3	SSYSADC[2]	B24	VSS	V4
EB_WDATA[60]	K4	SSYSADC[3]	A25	VSS	W23
EB_WDATA[61]	J3	SSYSADC[4]	C26	VSSA	A13
EB_WDATA[62]	H3	SSYSADC[5]	D24		
EB_WDATA[63]	J4	SSYSADC[6]	C25		

Table 30 Ball Assignments (ball order)

A1	VSS	AF11	EB_RDATA[12]	J23	VSS
A2	VSS	AF12	EB_RDATA[14]	J24	CVDD
A3	TR_TRIGOUT	AF13	EB_RDATA[15]	J25	EB_RDATA[59]
A4	CVDD	AF14	EB_RDATA[17]	J26	EB_RDATA[60]
A5	TIN[3]	AF15	EB_RDATA[18]	K1	IINT_N[1]
A6	TIN[1]	AF16	EB_RDATA[20]	K2	INMI_N
A7	TIN_N[3]	AF17	EB_RDATA[22]	K3	EB_WDATA[59]
A8	TIN_N[2]	AF18	EB_RDATA[24]	K4	EB_WDATA[60]
A9	TIN_N[0]	AF19	EB_RDATA[25]	K23	SSYSAD[13]
A10	SI_RESET	AF20	EB_RDATA[27]	K24	SSYSAD[12]
A11	SI_SIMPLEBE[0]	AF21	EB_RDATA[29]	K25	EB_RDATA[57]
A12	CVDD	AF22	EB_RDATA[31]	K26	EB_RDATA[58]
A13	VSSA	AF23	SSYSCMDP	L1	IINT_N[3]
A14	GBYPASS	AF24	SSYSAD[35]	L2	IINT_N[2]
A15	GCLK	AF25	VSS	L3	CVDD
A16	EB_EWBE	AF26	VSS	L4	VDD

Table 30 Ball Assignments (ball order) (Continued)

A17	GRST2_N	B1	PM_DTLBMISS	L11	VSS
A18	EB_SBLOCK	B2	VSS	L12	VSS
A19	PM_INSTNCOMPLETE	B3	TR_DATA[7]	L13	VSS
A20	PM_ICACHEHIT	B4	TR_DATA[4]	L14	VSS
A21	SWRRDY_N	B5	TIN[2]	L15	VSS
A22	GMULT[0]	B6	TIN[0]	L16	VSS
A23	GMULT[1]	B7	CVDD	L23	VDD
A24	SSYSADC[1]	B8	TIN_N[1]	L24	SSYSAD[14]
A25	SSYSADC[3]	B9	SVALIDIN_N	L25	EB_RDATA[55]
A26	VSS	B10	SI_MERGEMODE[1]	L26	EB_RDATA[56]
AA1	MBUS[0]	B11	PM_ITLBHIT	M1	IINT_N[5]
AA2	TR_TRIGIN	B12	VDDA	M2	IINT_N[4]
AA3	EB_WDATA[41]	B13	PLL_NC[2]	M3	EB_WDATA[57]
AA4	VDD	B14	GCLKB	M4	EB_WDATA[58]
AA23	VDD	B15	CVDD	M11	VSS
AA24	SSYSAD[26]	B16	EB_WBERR	M12	VSS
AA25	EB_RDATA[35]	B17	SEXTRQST_N	M13	VSS
AA26	EB_RDATA[36]	B18	SRDRDY_N	M14	VSS
AB1	MBUS[1]	B19	CVDD	M15	VSS
AB2	CSYSAD	B20	PM_ICACHEMISS	M16	VSS
AB3	EB_WDATA[38]	B21	SSYSCMD[4]	M23	SSYSAD[15]
AB4	EB_WDATA[39]	B22	SSYSCMD[7]	M24	SSYSAD[16]
AB23	SSYSAD[29]	B23	SSYSADC[0]	M25	EB_RDATA[53]
AB24	SSYSAD[28]	B24	SSYSADC[2]	M26	EB_RDATA[54]
AB25	EB_RDATA[33]	B25	VSS	N1	TSM
AB26	EB_RDATA[34]	B26	VSS	N2	TSI
AC1	CTIMER5	C1	ETRST_N	N3	EB_WDATA[54]
AC2	EB_WDATA[40]	C2	PM_DTLBHIT	N4	VSS
AC3	EB_WDATA[36]	C3	VSS	N11	VSS
AC4	VSS	C4	TR_CLK	N12	VSS
AC5	EB_WDATA[31]	C5	TR_DATA[6]	N13	VSS
AC6	VDD	C6	TR_DATA[3]	N14	VSS
AC7	EB_WDATA[29]	C7	TR_DATA[2]	N15	VSS
AC8	VSS	C8	TR_DATA[0]	N16	VSS

Table 30 Ball Assignments (ball order) (Continued)

AC9	SSYSAD[62]	C9	ERES[0]	N23	SSYSAD[18]
AC10	SSYSAD[59]	C10	PM_WTBNOMERGE	N24	CVDD
AC11	VDD	C11	PM_JTLBMISS	N25	EB_RDATA[51]
AC12	SSYSAD[56]	C12	PM_ITLBMISS	N26	EB_RDATA[52]
AC13	VSS	C13	PLL_NC[0]	P1	TSE
AC14	SSYSAD[54]	C14	LF	P2	EB_WDATA[56]
AC15	SSYSAD[50]	C15	CVDD	P3	EB_WDATA[53]
AC16	VDD	C16	EDINT	P4	EB_WDATA[55]
AC17	SSYSAD[48]	C17	PM_DCACHEMISS	P11	VSS
AC18	VSS	C18	SVALIDOUT_N	P12	VSS
AC19	SSYSAD[45]	C19	SRELEASE_N	P13	VSS
AC20	SSYSAD[43]	C20	SSYSCMD[1]	P14	VSS
AC21	VDD	C21	SSYSCMD[2]	P15	VSS
AC22	SSYSAD[39]	C22	SSYSCMD[5]	P16	VSS
AC23	VSS	C23	SSYSCMD[8]	P23	VSS
AC24	SSYSAD[30]	C24	VSS	P24	SSYSAD[17]
AC25	SSYSAD[31]	C25	SSYSADC[6]	P25	EB_RDATA[49]
AC26	EB_RDATA[32]	C26	SSYSADC[4]	P26	EB_RDATA[50]
AD1	EB_WDATA[35]	D1	ETCK	R1	CBIGEN
AD2	EB_WDATA[37]	D2	EJ_DEBUGM (TR_DM)	R2	MINP_N[0]
AD3	VSS	D3	SI_RP	R3	CVDD
AD4	EB_WDATA[32]	D4	VSS	R4	EB_WDATA[50]
AD5	EB_WDATA[30]	D5	TR_DATA[5]	R11	VSS
AD6	EB_WDATA[28]	D6	VDD	R12	VSS
AD7	SSYSAD[63]	D7	TR_DATA[1]	R13	VSS
AD8	SSYSAD[61]	D8	ERES[1]	R14	VSS
AD9	SSYSAD[60]	D9	VSS	R15	VSS
AD10	SSYSAD[58]	D10	PM_WTBMERGE	R16	VSS
AD11	SSYSAD[57]	D11	VDD	R23	SSYSAD[20]
AD12	SSYSAD[55]	D12	PM_JTLBHIT	R24	SSYSAD[19]
AD13	SSYSAD[53]	D13	PLL_NC[1]	R25	EB_RDATA[47]
AD14	SSYSAD[52]	D14	VSS	R26	EB_RDATA[48]
AD15	SSYSAD[51]	D15	GRST_N	T1	EB_WDATA[51]
AD16	SSYSAD[49]	D16	VDD	T2	EB_WDATA[52]

Table 30 Ball Assignments (ball order) (Continued)

AD17	SSYSAD[47]	D17	PM_DCACHEHIT	T3	EB_WDATA[49]
AD18	SSYSAD[46]	D18	SSYSCMD[0]	T4	VDD
AD19	SSYSAD[44]	D19	VSS	T11	VSS
AD20	SSYSAD[42]	D20	SSYSCMD[3]	T12	VSS
AD21	SSYSAD[41]	D21	VDD	T13	VSS
AD22	SSYSAD[38]	D22	SSYSCMD[6]	T14	VSS
AD23	SSYSAD[36]	D23	VSS	T15	VSS
AD24	VSS	D24	SSYSADC[5]	T16	VSS
AD25	SSYSAD[33]	D25	SSYSAD[2]	T23	VDD
AD26	SSYSAD[32]	D26	SSYSAD[0]	T24	SSYSAD[21]
AE1	VSS	E1	TSO	T25	EB_RDATA[45]
AE2	VSS	E2	CVDD	T26	EB_RDATA[46]
AE3	EB_WDATA[34]	E3	EJ_PERRST	U1	MINP_N[2]
AE4	EB_WDATA[33]	E4	SI_EXL	U2	MINP_N[1]
AE5	EB_RDATA[3]	E23	SSYSAD[1]	U3	EB_WDATA[47]
AE6	CPIPEWR	E24	SSYSADC[7]	U4	EB_WDATA[48]
AE7	CVDD	E25	CVDD	U23	SSYSAD[22]
AE8	EB_RDATA[6]	E26	EB_RDATA[63]	U24	CVDD
AE9	EB_RDATA[8]	F1	ETDO	U25	EB_RDATA[43]
AE10	EB_RDATA[10]	F2	ETMS	U26	EB_RDATA[44]
AE11	CVDD	F3	EJ_SRSTE	V1	CVDD
AE12	EB_RDATA[13]	F4	VDD	V2	TR_PROBE_N
AE13	CVDD	F23	VDD	V3	EB_WDATA[45]
AE14	EB_RDATA[16]	F24	SSYSAD[3]	V4	VSS
AE15	CVDD	F25	EB_RDATA[61]	V23	SSYSAD[25]
AE16	EB_RDATA[19]	F26	EB_RDATA[62]	V24	SSYSAD[23]
AE17	EB_RDATA[21]	G1	TOUT[0]	V25	EB_RDATA[41]
AE18	EB_RDATA[23]	G2	ETDI	V26	EB_RDATA[42]
AE19	CVDD	G3	CVDD	W1	MINP[0]
AE20	EB_RDATA[26]	G4	EJ_PRRST	W2	EB_WDATA[46]
AE21	EB_RDATA[28]	G23	SSYSAD[5]	W3	CVDD
AE22	EB_RDATA[30]	G24	SSYSAD[4]	W4	EB_WDATA[44]
AE23	SSYSAD[40]	G25	SSYSAD[9]	W23	VSS
AE24	SSYSAD[37]	G26	SSYSAD[7]	W24	SSYSAD[24]

Table 30 Ball Assignments (ball order) (Continued)

AE25	VSS	H1	TOUT[2]	W25	EB_RDATA[39]
AE26	SSYSAD[34]	H2	TOUT[1]	W26	EB_RDATA[40]
AF1	VSS	H3	EB_WDATA[62]	Y1	MINP[2]
AF2	EB_RDATA[0]	H4	VSS	Y2	MINP[1]
AF3	EB_RDATA[1]	H23	SSYSAD[8]	Y3	EB_WDATA[42]
AF4	EB_RDATA[2]	H24	SSYSAD[6]	Y4	EB_WDATA[43]
AF5	EB_RDATA[4]	H25	SSYSAD[11]	Y23	SSYSAD[27]
AF6	C4WBLK	H26	SSYSAD[10]	Y24	CVDD
AF7	EB_RDATA[5]	J1	TOUT[3]	Y25	EB_RDATA[37]
AF8	EB_RDATA[7]	J2	IINT_N[0]	Y26	EB_RDATA[38]
AF9	EB_RDATA[9]	J3	EB_WDATA[61]		
AF10	EB_RDATA[11]	J4	EB_WDATA[63]		

Notes:

- All pins named VSS are the pre-allocated VSS balls.
- All pins named VDD are the pre-allocated VDD balls (used for I/O buffers).
- All pins named CVDD are the core supply.
- The pins VSSA, VDDA are the PLL quiet analog supplies.

7.1 PLL Connections

There are 6 balls reserved for the analog connections to the PLL (quiet supplies, optional loop filter etc.). The connections to these 6 balls are different depending on the actual implementation of the LV.

The pinout in the previous section describes the “default” PLL pinout, but some of the LVs have different connections on these 6 balls. These implementation specific connections are discussed in the implementation chapter.

7.1.1 General PCB Design Rules for PLL Connections

In order to design a PCB which is generally usable with any LV, the following rules apply: on the PCB, each of the 6 pins allocated to analog PLL connections must have two 0805 passive components allocated, one connected to VSSA, one to VDDA. These components can be mounted with either capacitors or resistors. For any LV which uses A13 for the VSSA supply, the component to VSSA would be fitted with a 0 ohm resistor, whereas the component attaching to VDDA would be fitted with a decoupling capacitor.

The only pin which should have a different PCB layout is the C14 pin (LF). It must have three 0805 components, one to VSSA, and two other in series to VSSA. This allows the creation of the loop filter designs shown above.

The VDDA supply itself must be able to be configured to a filtered version of either the core supply voltage or the I/O buffer supply voltage. This can e.g. be accomplished by having two mount options for the inductor in the filter.

There is no guarantee that all future LV’s will be able to use this PCB layout, but MIPS will try to align the implementations to make this possible.

Appendices

A Revision History

Revision	Date	Description
01.00	99/05/12	Initial version. Created from the previous “Jade LV specification”
01.01	99/05/27	Added SysAD interface description.
01.02	99/08/12	Moved PM_* pins from SysAD tables to core bond-out tables. Changed load spec on PM_* pins from 50 to 25 pF. Added warning that MINN, MINP pins might become outputs on future devices.
01.03	99/10/25	Minor clarifications based on review feedback. Changed 5K LV cache & TLB spec. Added CSM 4K LV to tables. Made a new chapter collecting all the implementation specific specifications.
01.04	99/11/25	Changed all pin names to follow new convention. Replaced ERES[14] with EJ_DebugM. Suggested EJTAG pullups/downs changed to 1k (was 10k). EJTAG buffer drive capability changed to 8 mA (was 6mA). Changed VDDA for ID=1 to 3.3V (was 1.8V).
01.05	99/12/15	Restructured pin-tables to be more readable. Changed document to use new document template. Changed “Jade” and “Opal” names to 4K/5K. Replaced ERES[13] and ERES[12] with two new dedicated performance monitoring pins PM_DTLBHit and PM_DTLBMiss for use on the 5K LV.
01.06	00/03/30	Changed formatting of EJTAG timing spec. Added notes in a few places referring readers to the LV ”Specification Update” documents.
01.07	00/06/09	Updated relevant J25C1 silicon information in chapter 6. Added GCLKB output timing to AC timing table. New versions of 4K LV’s now support 3x,4x clock multipliers as well. Added description of SysAD64 address behavior for single accesses in normal and reverse endian modes.
01.08	01/01/18	Conversion to new document template. Added information on LSS LJA0004 LV.
01.09	01/06/21	Added descriptions of 4KE/4KS and 5Kf cores where relevant. Many changes throughout the document to describe the changes around SI_MergeMode and SI_SimpleBE (function and name change vs. previous versions). Changed required GCLKB timing window from [-1;1] to [-2;0] to ease board bringup in PLL bypass modes.
01.10	01/07/27	Added PDtrace pins to the LV. These new pins replace previously reserved pins on the LV. The new pins are: TR_Probe_n (previously MINP_N[3]), TR_TrigIn (previously MINP[3]), TR_TrigOut (previously ERES[11]), TR_Clk (previously ERES[10]) and TR_Data[7:2[(previously ERES[9:2]). Added the TR_DM pin alias name for the EJ_DebugM pin (relevant only for LV’s supporting PDtrace). Added TI 5KC LV silicon data (ID: 4) to Chapter 6. Redid pin/ball assignment tables to make them truly alfabetic.